Effect of Output Buffer Design on 40Gb/s Limiting Amplifiers Designed with InP HBT Technology

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Abstract **-- An InP-based HBT technology with peak f_t~135GHz is used to design and fabricate several 3-stage limiting amplifier with high margin at >40Gbps. Feedback techniques are used in all design for the first two stages. The different designs compare the conventional (resistive load) differential pair output buffer with a feedback (active load) transimpedance output buffer. The common differential specifications are S11 and S22 < -15dB and S21 > 25dB with output swing >500mV. Results show that the design with the negative feedback output buffer has a lower small-signal bandwidth but a larger 40Gb/s eye opening than design with the conventional differential pair output buffer.**

1. INTRODUCTION

One of the analog circuits required by the lightwave system receiver is the limiting amplifier with a high gain-bandwidth product. High gain is needed to make a reliable decision in the presence of system noise, from the <50mV signal from the proceeding detector through the transimpedance amplifier to about the full ECL logic swing. High bandwidth is needed to pass higher order harmonics of the rise and fall times. Differential design improves common mode rejection.

Several 3-stage limiting amplifier are designed to compare the conventional resistive load differential pair output buffer with a feedback active load transimpedance output buffer. The first two stages of all designs cascade transadmittance - transimpedance blocks (Cherry - Hooper [1,2] feedback design) to obtain higher bandwidth. All limiting amplifiers are designed to the common single-ended specifications of input reflection (S11) and output reflection (S22) < -10dB and gain (S21) > 20dB with output swing ~400mV.

Circuit fabrication uses an InP double heterojunction bipolar transistor D-HBT technology [3,4,5] with peak f_T ~ 140GHz. Small signal and limiting transient responses are obtained with on-wafer probing.

Below we discuss the InP HBT process technology, circuit design, physical layout and measurement results.

2. PROCESS TECHNOLOGY

The all-optical lithography InGaAs / InP D-HBT process technology [3,4,5], is used for the design and fabrication of the limiting amplifier. The D-HBT layer structure is grown using metal-organic molecular beam epitaxy (MOMBE) with carbon doping in the ~500Å thick base for improved reliability. The basic transistor has an as-drawn emitter area of 1.2x3.0 μm^2 which is undercut to ~1.0x2.8 μm^2 to facilitate the self-aligned Au metalization by liftoff. Figure 1 shows f_t and f_{max} at V_{CE}=1.5V, as a function of collector current. The f_t peak is relatively broad at 100-150kA.cm^2. Note that the f_t is relatively insensitive to V_{CE} as long as V_{CE}>1V. Lower V_{CE} gives correspondingly lower RF performance.

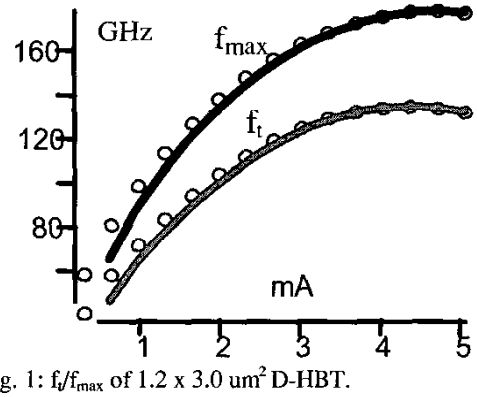

Fig. 1: f_t/f_{max} of 1.2 x 3.0 um^2 D-HBT.
Peak f_t/f_{max} = 135 / 180GHz at ~4mA.

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The first two stages of the limiting amplifier design use the slightly relaxed 1.6x3.4 μm^2 as-drawn emitter. The output buffer uses a 1.6x7 μm^2 device to provide the required output swing. The devices are DC biased at 100kA/cm^2 to further improve on circuit yield and reliability.

For design simulations, the basic transistor is described with a Gummel-Poon model. The optimized feedback circuit design compensated poles related to junction (primarily base-collector) capacitance. For the 1.6 x 3.4 μm^2 D-HBT used for the amplifier designs, the mesa structure R_b=48Ω, R_e=9Ω, R_c=19Ω, C_{je0}~7fF and C_{jc0}~15.4fF. The ratio of the intrinsic to extrinsic device (~ emitter to base area describing the fringing field effects) is XCJC ~ 0.25. The RF data is de-embedded before extracting the device model.

The technology uses mesa isolation to the InP substrate. Mesa heights are ~1.5μm. The mesas are planarized and passivated with bisbenzocyclobutene (BCB). The standard process includes 1½ levels of gold metalization (M0 for local interconnect and M1 for longer-range interconnect). Vias are etched, filled and planarized by liftoff to obtain interlevel connections. The process has NiCr resistors and Si_3N_4 MIM capacitors.

3. CIRCUIT DESIGN AND LAYOUT

The amplifier design criteria are (1) fully differential circuits with single power supply (-Vee), (2)>20dB single-ended gain, (3) >40GHz bandwidth, (4) S11 and S22 <-10dB, and (5) >250mV single-ended output. Gain peaking of the small signal response, is <1dB to minimize group delay. Circuit speed, implying near-maximum transistor current density at sufficient transistor V_{CE}, is an important factor in this design.

The limiting amplifier circuit architecture [6,7,8] is shown in Fig. 2. Three stages are cascaded. The first two stages are of the Cherry-Hooper design for which the component level schematic is shown in Fig. 3. The component level schematics of the conventional resistive load differential pair and the feedback active load transimpedance output buffer are shown in Fig 4.

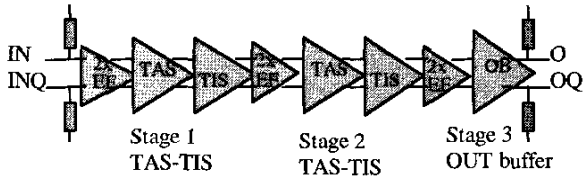

Fig. 2: Limiting amplifier architecture. Three stages (2 stages transadmittance-transimpedance TAS-TIS and output buffer OUT) cascaded with intermediate 2 emitter follower 2xEF level shift. 50Ω on-chip termination at IN and OUT.

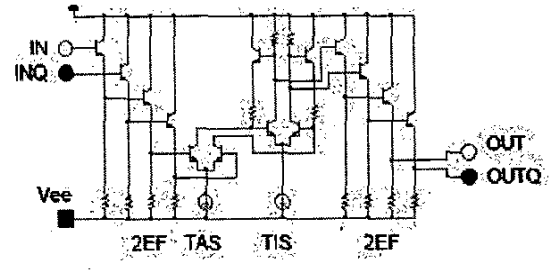

Fig. 3. Core amplifier Cherry-Hooper TAS-TIS cell with 2 emitter-follower level shift for cascading.

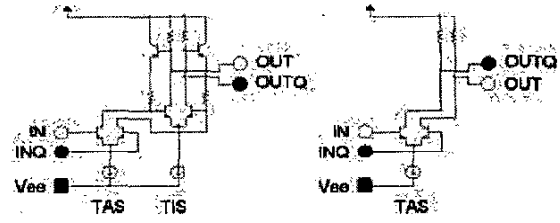

Fig. 4. Output buffer design. Conventional resistive load differential pair output buffer (right) compared with the feedback (active load) transimpedance output buffer (left).

Differential emitter coupled logic blocks with two emitter follower level shifts (E^2CL) are used for the basic amplifier cell. To improve high frequency performance, the TAS-TIS combination connected with coupled coplanar transmission lines is also used for the basic amplifier cell. Using the TIS active load provides a higher gain-bandwidth products than from the conventional resistor load.

Only the one transistor size (1.6 x 3.4μm^2) is used in the standard cell. Therefore, the cell bandwidth is optimized by choosing (1) the appropriate feedback resistor value to compensate transistor junction capacitance, (2) the appropriate load resistor value to use the minimum required internal voltage swing and (3) the various tail currents =100kA/cm^2 in each tail current transistor. Typical internal differential voltage swings are ~400mV. The current is established in the current mirrors with one simple current source for each of the Cherry-Hooper stages and another for the output buffer. The current in the output stage is set by the desired voltage swing. A larger 1.6 x 7um^2 transistor is needed the differential pair (labeled TAS in Fig. 4) to obtain the design specification of >250mV single-ended into 50Ω.

Figure 5 shows chip photographs of the limiting amplifiers with the feedback active load transimpedance (left) and conventional resistive load (right) output

buffers. To simplify the layout process at high bitrate, standardized analog blocks were designed and reused with only minor changes in the passive component values.

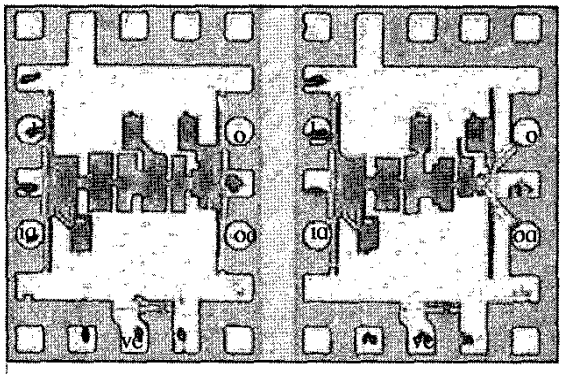

Fig. 5: Chip photographs of limiting amplifier with TIS (left) and NO TIS (right) output buffer.

This can be seen from the nearly identical layouts, except for the addition of the TIS stage at the output buffer in the left chip. Matching delays for the complimentary signal paths, was achieved by symmetric layout. Coplanar and microstrip transmission lines with controlled impedance, are used for the longer (>lambda/10) interconnects in the signal path. Lines driven by emitter followers are kept short to minimize reflections due to impedance mismatch.

An on-chip de-coupling RC network is used to bypass V_{EE} so as to avoid any spurious oscillations that could arise in the packaged IC. The chips nominally consume ~120mA with a single bias of V_{EE} ~ -5.5V.

The input and output are DC coupled (near 0V). DC offset tuning is provided by a high resistance connection to the input and output. The chip area is pad limited at 675 x 975 μm^2.

4. TEST RESULTS

Figure 6 shows typical small signal S-parameter data. The feedback and conventional output buffer variations are respectively at left and right. Results are derived from single-ended on-wafer probing.

The gain peaking has a different frequency dependence for the feedback and conventional output buffer variations. The conventional output buffer variation has a 10% larger bandwidth than the feedback output buffer variation (46GHz vs. 42GHz). Also, the output reflection (S22) is higher for the TIS variation but still below the design goal of <-10dB.

Figure 7 shows typical limiting eye diagrams. The feedback and conventional output buffer variations are respectively at top and bottom. Results are derived from single-ended on-wafer probing. The input data was single-ended 60mV, 40Gb/s 2^{31}-1 PRBS. Input offset for the unused input is needed to correct the zero-crossing and to obtain an open eye.

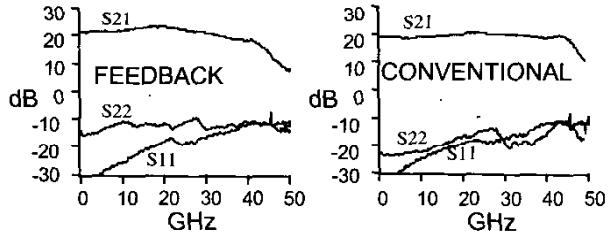

Fig. 6: Measured S21, S11 and S22 for feedback (left) and conventional (right) output buffer variations. Single-ended in/out. The differential gain is 26dB.

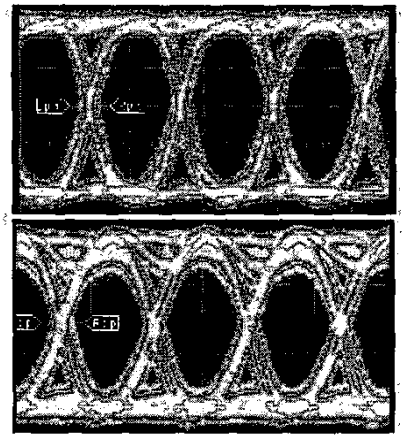

Fig. 7: Single-ended eye diagrams. Feedback (top) and conventional (bottom) output buffer variations.

Open 40Gb/s eyes with output magnitude ~400mV into 50Ω, are measured for both variations. The feedback output buffer variation has better large signal response (more open eye). Lower jitter and less ripple is observed correlating with lower peaking of the small-signal response (Fig. 6) near the high frequency cutoff.

5. DISCUSSION

The design difference between the circuits with feedback or conventional output buffer is the output buffer type. (Simulation shows that the small signal gain is the same up to the output buffer, for both designs.) Specifically, the gain peaking associated with the negative feedback of the first two amplifier stages, is kept small

(~1dB) to avoid unstable oscillation. But, some peaking exists to increase bandwidth.

In the conventional output buffer design, the convolution of the small signal gain characteristic of the conventional resistive load differential pair output buffer can only decrease the peaking near the gain roll-off. However, in the present conventional output buffer design, some final gain peaking near 40GHz, remains in order to have some enhancement of the bandwidth.

In the feedback output buffer design, the active load introduces additional negative feedback. The placement of negative feedback zero of the buffer stage, will have a controlling effect on the final small signal gain. Placing the buffer zero near the gain roll-off of the first two stages increases peaking. Placing the buffer zero away from the gain roll-off of the first two stages decreases peaking. In the present feedback output buffer design, the final gain peaking is almost eliminated at ~40GHz by enhancing the broad gain peaking at 20GHz.

Small-signal gain peaking (~1-2dB) is associated with large-signal damped oscillation. Narrow peaking will appear in the large signal eye diagram, as ringing. Broad peaking is not as obvious in the eye diagram, because of phase-frequency addition.

Thus, the damped oscillation at 40GHz is obvious in the eye diagram of the design with the conventional output buffer (Fig. 7 bottom). This peaks the single bit of the 40Gb/s PRBS pattern and reduces the magnitude of second "1" of the double bit in the 40Gb/s PRBS pattern. Thus, damped oscillation associated with gain peaking in the design with the conventional output buffer, results in a less-open eye with less hard limiting.

6. CONCLUSION

Several limiting amplifier designs with an InP-based process with ft / fmax = 135 / 180GHz, showed good small and large signal performance at 40Gb/s. Replacing the conventional resistive load differential pair output buffer with a feedback (active load) transimpedance output buffer improves on the large-signal performance (eye opening, jitter and hard limiting) by allowing for control of the frequency location of the gain peaking away from the small-signal gain roll-off. This can decrease small-signal performance which is less relevant for limiting amplifier applications.

REFERENCES

[1] E. M. Cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifier", Inst. Elec. Eng. Proc., vol.110, no.2, pp.375-389, Feb. 1963.

[2] H.-M.Rein and M.Moeller, "Design Considerations for Very-Hlgh-Speed Si-Bipolar IC's Operating up to 50Gb/s." IEEE J. Solid State Circuits, vol. 31, p. 1076-1090, August 1996.

[3] R.F.Kopf, R.Hamm, R.Ryan, A.Tate, R.Pullela, G.Georgiou, J.-P.Mattia and Y.-K.Chen, "Dry –etch Fabrication of Reduced Area InGaAs/InP HBTs." J. Electron. Mat., vol. 29, no. 2, p. 222, 2000.

[4] R.F.Kopf, R..A.Hamm, R.W.Ryan, J.Burm, A.Tate, Y.-K.Chen, G.Georgiou, J.-P.Mattia and Y.-K.Chen, "Dry –etch Fabrication of Reduced Area InGaAs/InP HBTs." J. Electron. Mat., vol. 29, p. 222, 2000.

[5] Y.Yang, J.Frackoviak, C.T.Liu, C.J.Chen, L.-L.Chua, W.J.Sung, A.Tate, J.Tong, R.Reyes, R.Kopf, R.Ruel, D.Werder, V.Houtsma, G.Georgiou, J.S.Weiner, Y.Baeyens and Y.-K.Chen, "High-Performance and High-Uniformity InP/InGaAs/InP DHBT Technology for High-Speed Optical Communication Systems." IEEE GaAs IC Symp. Tech. Dig., 2002, pp 269-272.

[6] G. Georgiou, Y.Baeyens, Y.-K.Chen, A.H.Gnauck, C.Gröpper, P.Paschke,R.Pullela, M.Reinhold, C.Dorschky, J.-P.Mattia, T.W.von Mohrenfels and C.Schulien, "Clock and Data Recovery IC for 40Gb/s Fiber-Optic Receiver." IEEE J. Solid-State Circuits, vol . 37, pp. 1120-1125, Sept. 2002.

[7] M.Reinhold, C.Dorschky, R.Pullela, E.Rose, P.Mayer, P.Paschke, Y.Baeyens, J.-P.Mattia, and F.Kunz, "A fully integrated 40Gb/s clock and data recovery / 1:4 DEMUX IC SiGe technology." IEEE J. Solid-State Circuits, vol . 36, pp. 1937-1945, Dec. 2001.

[8] Y.Baeyens , G. Georgiou, J.S.Weiner, A.Leven, V.Houtsma, P.Paschke. Q.Lee, R.F.Kopf, Y.Yang, L.Chua, C.Chen, C.T.Liu and Y.-K.Chen. "InP D-HBT Ics for 40Gb/s and Higher Bitrate Lightwave Tranceivers." IEEE J. Solid-State Circuits, vol . 37, pp. 1152-1159, Sept. 2000.